CERTIFICATE OF TRANSLATION

I, the undersigned, hereby certify

that I am well acquainted with the English and Japanese languages,

that I prepared the attached document, and

that, to the best of my knowledge and belief, the attached document is an accurate translation of Japanese patent application No. 2004-120168 filed on April 15, 2004.

I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true.

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Date

[Name of the Document] Claims

[Claim 1] A semiconductor integrated circuit used for data carriers in contactless type information system in which communications between a reader/writer and the data carriers, the semiconductor integrated circuit comprising:

a memory circuit section; a logic circuit section; a rectifier circuit section; and a first reset generating circuit section, wherein

the memory circuit section stores data to be exchanged with the reader/writer,

the logic circuit section has a function of obtaining the data stored in the memory circuit section to transmit the data to the rectifier circuit section when a first signal is not transmitted from the first reset generating circuit section, and a function of transmitting a second signal to the first reset generating circuit section when the data stored in the memory circuit section is transmitted to the rectifier circuit section,

the rectifier circuit section rectifies the data transmitted from the logic circuit section to transmit the rectified data to the reader/writer, and

the first reset generating circuit section does not transmit the first signal to the logic circuit section when the logic circuit section transmits the data stored in the memory circuit section to the rectifier circuit section.

[Claim 2] A semiconductor integrated circuit used for data carriers in contactless type information system in which communications between a reader/writer and the data carriers, the semiconductor integrated circuit comprising:

a memory circuit section; a logic circuit section; a rectifier circuit section; and a first reset generating circuit section, wherein

the memory circuit section stores data to be exchanged with the reader/writer,

the logic circuit section has a function of obtaining the data stored in the memory circuit section to transmit the data to the rectifier circuit section when a first signal is not transmitted

from the first reset generating circuit section, and a function of transmitting a second signal to the first reset generating circuit section when the data stored in the memory circuit section is transmitted to the rectifier circuit section,

the rectifier circuit section rectifies the data transmitted from the logic circuit section to transmit the rectified data to the reader/writer, and

the first reset generating circuit section decreases a power supply voltage with a first series of resistors, compares the decreased voltage with a predetermined first reference voltage, and transmits the first signal to the logic circuit section when the decreased voltage is lower than the predetermined first reference voltage.

[Claim 3] The semiconductor integrated circuit of claim 2, wherein

the first reset generating circuit section increases the decreased voltage when the second signal is transmitted from the logic circuit section.

[Claim 4] The semiconductor integrated circuit of claim 2 or claim 3, wherein

the first reset generating circuit section has a function of reducing the number of resistors constituting the first series of resistors for decreasing the power supply voltage when the second signal is transmitted from the logic circuit section.

[Claim 5] The semiconductor integrated circuit of any of claims 1 though 4, wherein

the logic circuit section starts to transmit the data stored in the memory circuit section to the modulator circuit, while starts to transmit the second signal to the first reset generating circuit section.

[Claim 6] The semiconductor integrated circuit of any of claims 1 though 5, wherein

the logic circuit section, before transmitting the data stored in the memory circuit section to the rectifier circuit, stores the data to be transmitted in a buffer, and

the logic circuit section does not obtain the data stored in the memory circuit section when transmitting the data stored in the memory circuit section to the rectifier circuit section.

[Claim 7] The semiconductor integrated circuit of any of claims 1 though 6, wherein

the logic circuit section delays a timing of completing the transmission of the second signal to the first reset generating circuit section with respect to a timing of completing the transmission of the data stored in the memory circuit section to the rectifier circuit, by a delay amount which is longer than a period in which the transmission of the data stored in the memory circuit section to the rectifier circuit is completed.

[Claim 8] The semiconductor integrated circuit of any of claims 1 though 7, further comprising

a second reset generating circuit section which does not transmit the first signal to the logic circuit section when the logic circuit section transmits the data stored in the memory circuit section to the rectifier circuit section, wherein

the logic circuit section has a function of obtaining the data stored in the memory circuit section when a first signal is not transmitted from the first reset generating circuit section and the second reset generating circuit section, and a function of transmitting the second signal to the first reset generating circuit section and the second reset generating circuit section when the data stored in the memory circuit section is transmitted to the rectifier circuit section.

[Claim 9] The semiconductor integrated circuit of any of claims 1 though 8, wherein

the second reset generating circuit section decreases a power supply voltage with a second series of resistors, compares the decreased voltage with a predetermined second reference voltage, and transmits the first signal to the logic circuit section when the decreased voltage is higher than the predetermined second reference voltage, and increases the decreased voltage when the logic circuit section transmits the data stored in the memory circuit section to the rectifier circuit section.

[Claim 10] The semiconductor integrated circuit of claim 9, wherein

the second reset generating circuit section reduces the number of resistors constituting

the second series of resistors for decreasing the power supply voltage when the logic circuit section transmits the data stored in the memory circuit section to the rectifier circuit section.

[Claim 11] A contactless type information system including the semiconductor integrated circuit of any of claims 1 through 10.

[Name of the Document] Specification

[Title of the Invention] SEMICONDUCTOR INTEGRATED CIRCUIT AND NONCONTACT INFORMATION SYSTEM INCLUDING IT

[Field of the Invention]

The present invention relates to a semiconductor integrated circuit and a system including a contactless type information medium including the semiconductor integrated circuit.

[Description of Related Art]

Recently, data carriers such as contactless IC cards, which are capable of transmitting and receiving data while receiving power supply at the same time by using electromagnetic waves of a predetermined wavelength utilizing the mutual induction between coils, have reached the stage of practical application. Contactless IC cards are classified into the close-coupled type, the proximity type and the vicinity type based on the reading range between the contactless IC card and the reader/writer, which is a device for exchanging radio waves with the contactless IC card. The standard specification for each type is being fully prepared.

Particularly, proximity type contactless IC cards, which can be used over a distance of up to about 10 [cm] from the reader/writer, are often used in applications such as train passes. The ticket gate in a station can be opened and closed based on the contactless exchange of information with the reader/writer, wherein the users do not need to take their train passes (contactless IC cards) out of the train pass holders at the ticket gate, or the like. Thus, contactless IC cards can potentially be used in a very wide variety of applications (See, for example, Patent Document 1.)

However, generally, if the voltage caused by the mutual induction between coils drops, it may disable communications between the contactless IC card and the reader/writer. In this way, one reason for the drop of the voltage generated in the coils is probably due to the

physical distance between the contactless IC card and the reader/writer being excessive. The voltage through the coil temporarily drops during the period in which data is being returned from the contactless IC card to the reader/writer after the data is transmitted from the reader/writer to the contactless IC card, even if the physical distance between the contactless IC card and the reader/writer is not excessive. Therefore, the data communications between the contactless IC card and the reader/writer becomes unstable. The contactless IC card has a predetermined reset detection lower limit voltage. When the voltage generated in the coil becomes lower than a predetermined reset detection lower limit voltage, the data communications between the contactless IC card and the reader/writer may constantly be reset even in the middle of a data exchange, thus failing to exchange data between the contactless IC card and the reader/writer.

[Patent Document 1] Japanese Laid-Open Patent Publication No. 8-77318

[Disclosure of the invention]

[Problems that the invention is to solve]

It is an object of the present invention to provide a semiconductor integrated circuit having a simple circuit configuration, allowing the reading range between a contactless IC card and a reader/writer to extend, and ensuring stable communications without increasing a size of the contactless IC card (contactless type information medium).

[Means For Solving The Problems]

In order to achieve the object, a semiconductor integrated circuit for data carriers regarding one aspect of the present invention comprises a memory circuit section, a logic circuit section, a rectifier circuit section, and a reset generating circuit section. The memory circuit section stores data to be exchanged with the reader/writer. The logic circuit section has a function of obtaining data stored in the memory circuit section to transmit the data to the rectifier circuit section when a first signal is not transmitted from the reset generating circuit section, and

a function of transmitting a second signal to the reset generating circuit section when the data stored in the memory circuit section is transmitted to the reader/writer. The rectifier circuit section has a feature of rectifying data transmitted from the logic circuit section to transmit the rectified data to the reader/writer. The reset generating circuit section has a feature of not transmitting the first signal to the logic circuit section when the logic circuit section transmits the data stored in the memory circuit section to the rectifier circuit section.

A reset generating circuit section existing in a semiconductor integrated circuit for data carriers regarding another aspect of the present invention decreases a power supply voltage with a series of resistors, and compares the decreased voltage with a predetermined reference voltage. When the decreased voltage is lower than the predetermined reference voltage, the reset generating circuit section has a function of transmitting the second signal to the logic circuit section. Further, when the second signal is transmitted from the logic circuit section to the reset generating circuit section, a function of reducing the number of resistors constituting the series of resistors for decreasing the power supply voltage may be added to the reset generating circuit section. These functions are similar to functions of the reset generating circuit section of comparing the reset detection lower limit voltage and the power supply voltage, and transmitting the signal to the logic circuit section when the power supply voltage is lower than the reset detection lower limit voltage, and decreasing the reset detection lower limit voltage when the signal is transmitted from the logic circuit section.

A semiconductor integrated circuit for data carriers regarding another aspect of the present invention further includes another reset generating circuit section having a function of compares the decreased voltage with a predetermined reference voltage, and transmitting a signal to the logic circuit section when the decreased voltage is higher than the predetermined reference voltage, and reducing the number of resistors constituting the series of resistors for decreasing a power supply voltage when the signal is transmitted from the logic circuit section.

[Effects of the Invention]

A semiconductor integrated circuit of the present invention does not stop an operation of the logic circuit section due to the decrease of the power supply voltage when the logic circuit section transmits data stored in the memory circuit section to the reader/writer, thus, data is returned from the contactless IC card to the reader/writer. Specifically, the semiconductor integrated circuit includes a reset detection lower limit voltage, and does not generate a reset signal due to the decrease of the power supply voltage Vdd occurring during the return of data since the semiconductor integrated circuit decreases the reset detection lower limit voltage when the data is returned from the contactless IC card to the data carrier. Therefore, communication distance between the contactless IC card and the data carrier can be extended, thereby ensuring stable data communications.

Further, a reset detection upper limit voltage is set, thereby making it difficult for a third person, with malicious intent, to read out, or overwrite data stored in the IC card. Therefore, this substantially improves the security of the IC card.

Therefore, Thus, the semiconductor integrated circuit of the present invention is useful in the application to contactless IC cards of the proximity type (reading range: 0 to 10 cm) expected to be widespread in the near future.

[Description of the Preferred Embodiments]

An embodiment of the present invention will now be described. FIG. 1 is a schematic view showing a contactless IC card system.

When a contactless IC card 1 is brought close to a reader/writer 2, data can be exchanged therebetween by using electromagnetic waves even in a non-contact state. The data exchange is performed through a protocol in which the reader/writer 2 transmits data to the contactless IC card 1 and then the contactless IC card 1 returns data to the reader/writer 2. As a result of the data exchange, the reader/writer 2 can obtain data, such as personal information,

stored in the memory of the contactless IC card 1. If the reader/writer 2 communicates with the host device 3, data stored in the contactless IC card 1 can be used for a wide variety of purposes.

A block configuration including the contactless IC card 1 and the reader/writer 2 is as shown in FIG. 2.

The contactless IC card 1 includes a contactless IC card LSI 11, an antenna coil 12 and a tuning capacitor 13. The contactless IC card LSI 11 includes an analog circuit section 20, a logic circuit section 21, a non-volatile memory circuit section 22, and the like.

The antenna coil 12 for transmitting and receiving electromagnetic waves 5 output from an antenna coil 4 of the reader/writer 2 is connected to the coil terminals 36 and 37 of the contactless IC card LSI 11, and the tuning capacitor 13 is connected to the antenna coil 12. Therefore, the antenna coil 12 receives electromagnetic waves 5 from the reader/writer 2, and therefore, an alternating-current voltage is generated between the coil terminal 36 and the coil terminal 37 of the antenna coil 12.

The alternating-current voltage generated between the coil terminal 36 and the coil terminal 37 of the antenna coil 12 is input into an analog circuit section 20. The analog circuit section 20 includes a rectifier circuit 30, a power supply circuit 31, a clock generating circuit 32, a demodulator circuit 33, a modulator circuit 34, and a reset generating circuit 35.

The rectifier circuit 30 rectifies the alternating-current voltage generated between the coil terminals 36 and 37 of the antenna coil 12 into a direct-current voltage, and stabilizes the voltage. The power supply circuit 31 transmits a power supply voltage Vdd, which has been rectified by the rectifier circuit 30, to the entire contactless IC card LSI 11. This enables the entire contactless IC card LSI 11 to operate.

The reset generating circuit 35 switches a reset signal RESET to be transmitted into the logic circuit section 21, depending on the level of the power supply voltage Vdd output from the power supply circuit 31, and thereby controlling data communications between the contactless

IC card 1 and the reader/writer 2. Specifically, the reset generating circuit 35 receives the power supply voltage Vdd from the power supply circuit 31, and when a level of the power supply voltage Vdd reaches a voltage level that the contactless IC card LSI 11 will not undergo an erroneous operation, the reset signal RESET is switched from a High level (H level) to a Low level (L level). When the reset signal RESET is at the High level, the logic circuit section 21 does not transmit a control signal Ctrl to the non-volatile memory circuit section 22. At that time, the logic circuit section 21 cannot access to non-volatile memory circuit section 22. On the contrary, when the reset signal RESET is at the Low level, the logic circuit section 21 transmits a control signal Ctrl to the non-volatile memory circuit section 22, thereby allowing the logic circuit section 21 to access to non-volatile memory circuit section 22. Therefore, the instance of the transition of the reset signal RESET from the H level to the L level is when the access to the non-volatile memory circuit section 22 is allowed. When the access to the non-volatile memory circuit section 22 is being allowed, the logic circuit section 21 can obtain data stored in the non-volatile memory circuit section 22. This not only allows an external device such as the reader/writer 2 to transmit data to the contactless IC card, but also allows the contactless IC card 1 to return data stored in the non-volatile memory circuit section 22 to the reader/writer 2.

The clock generating circuit 32 receives the alternating-current voltage generated between the opposite ends of the antenna coil 12 to generate a clock signal CLK, and outputs the clock signal CLK to the logic circuit section 21.

Data, which is transmitted when the reader/writer 2 transmits data to the contactless IC card 1, is rectified by the rectifier circuit 30, and then, the data is demodulated by the demodulator circuit 33. The demodulator circuit 33 tramsmits the demodulated signal RXDATA to the logic circuit section 21.

On the contrary, when the contactless IC card 1 returns data to the reader/writer 2, the

logic circuit section 21 switches a return signal TXDATA from the H level to the L level to the modulator circuit 34. Then, the modulator circuit 34 modulates the return signal TXDATA and transmits the modulated signal between the coil terminals, thereby returning the data from contactless IC card 1 and the reader/writer 2.

The logic circuit section 21 transmits an address signal Add to the non-volatile memory circuit section 22, thereby obtaining a data signal DATA corresponding to the address. The logic circuit section 21 transmits the address signal Add and the data signal DATA to the non-volatile memory circuit section 22, thereby storing data into the non-volatile memory circuit section 22.

FIG. 3 is a diagram showing a configuration of the antenna coil 12, the tuning capacitor 13, the coil terminals 36 and 37, the modulator circuit 34, and the rectifier circuit 30 of the contactless IC card 1. First, the antenna coil 12 provided in the contactless IC card 1 receives the electromagnetic waves 5 transmitted from the reader/writer 2. Then, the alternating-current voltage generated between the both ends of the antenna coil 12 is changed by a modulation transistor 82 and a modulation factor adjusting resistor 81 included in the modulator circuit 34. In other words, the load of the contactless IC card 1 varies. Then, the data is returned from the contactless IC card 1 to the reader/writer 2. During the period in which the data is returned from the contactless IC card 1 to the reader/writer 2, i.e., during the period in which the return signal TXDATA is at the L level, the modulation transistor 82 of the modulator circuit 34 is ON, and the voltage between the coil terminals 36 and 37 decreases. The contactless IC card 1 generates the power supply voltage Vdd with the voltage between the coil terminals 36 and 37.

However, when the voltage between the coil terminals 36 and 37 is sufficiently high (e.g., when the contactless IC card 1 and the reader/writer 2 are close to each other) or when the resistance value of the modulation factor adjusting resistor 81 of the modulator circuit 34 is sufficiently large, the supplied power is high even if the modulation transistor 82 is ON, whereby

there is little decrease in the voltage between the coil terminals 36 and 37. Therefore, there is little decrease in the power supply voltage Vdd, and the reset signal RESET will not be generated, thereby allowing data communications between the contactless IC card 1 and the reader/writer 2.

On the contrary, as the voltage between the coil terminals 36 and 37 is lower (e.g., as the contactless IC card 1 and the reader/writer 2 are spaced apart from each other) or as the resistance value of the modulation factor adjusting resistor 81 of the modulator circuit 34 is smaller, it is more likely that the power supply voltage Vdd decreases when the modulation transistor 82 of the load modulation type modulator circuit 34 is turned ON. Then, when the reset generating circuit 35 detects the decrease in the power supply voltage Vdd and outputs the reset signal RESET to the contactless IC card LSI 11, the entire contactless IC card LSI 11 stops operating. When the operation of the contactless IC card LSI 11 stops, it is no longer possible to perform data communications between the contactless IC card 1 and the reader/writer 2.

Therefore, if the resistance value of the modulation factor adjusting resistor 81 of the modulator circuit 34 is set to be small and if the modulation transistor 82 is ON (if the return of the data is performed from the contactless IC card 1 to the reader/writer 2), even though the voltage between the coil terminals 36 and 37 is not small, it becomes impossible to perform data communications between the contactless IC card 1 and the reader/writer 2.

Typically, the characteristics of the modulator circuit 34 are represented by the modulation factor, which indicates the data communications capability between the contactless IC card 1 and the reader/writer 2, as shown in FIG. 4. The standard of the modulation factor is specified in the international standard ISO/IEC 14443-2 regarding contactless IC cards. In order to satisfy the standard, the modulation factor of the contactless IC card 1 needs to be present within the region above the solid line (1) ($30/H^{1.2}$ [mVp]) in FIG. 4. Typically, the weaker the magnetic field intensity is, the smaller the voltage generated in the contactless IC card 1 is. Therefore, it is necessary to increase the modulation factor in order to enable data

communications between the contactless IC card 1 and the reader/writer 2. However, as indicated by the solid line (2) and the solid line (3) in FIG. 4, the magnitude of the modulation factor, i.e., the characteristics of the LSI 11, is not substantially dependent on the magnetic field intensity, i.e., the voltage generated between the coil terminals 36 and 37, but is dependent on the resistance value of the modulation factor adjusting resistor 81 of the modulator circuit 34. Therefore, it is possible to increase the modulation factor to such an extent that it is possible to sufficiently enable data communications between the contactless IC card 1 and the reader/writer 2, even when the magnetic field intensity is low. In order to increase the modulation factor, as stated above, the modulation factor adjusting resistor 81 of the modulator circuit 34 needs to have a small resistance value. However, if the modulation factor adjusting resistor 81 of the modulator circuit 34 is small, the power supply voltage Vdd is significantly decreased when the magnetic field intensity is low, and the return signal TXDATA from the logic circuit section 21 to the modulator circuit 43 is low, in other words, the data is returned from the contactless IC card 1 to the reader/writer 2. At that time, the reset generating circuit section 35 transmits the reset signal RESET to the logic circuit section 21, thereby making it impossible to perform data communications between the contactless IC card 1 and the reader/writer 2.

In summary, when the resistance value of the modulation factor adjusting resistor 81 is smaller, the modulation factor is higher, but the power supply voltage is decreased by a larger amount when data is returned from the contactless IC card 1 to the reader/writer 2. When the resistance value of the modulation factor adjusting resistor 81 is larger, the power supply voltage is decreased by a smaller amount when data is returned from the contactless IC card 1 to the reader/writer 2, but the modulation factor is smaller where the magnetic field intensity is low.

In the contactless IC card system according to the embodiment, the modulation factor adjusting resistor 81 having a small resistance value is used. The contactless IC card system according to the embodiment has a feature that, whenever data is returned from the contactless

IC card 1 to the reader/writer 2, the logic circuit section 21 transmits the switch signal SW to the reset generating circuit section 35. The logic circuit section 21 transmits the switch signal SW, and therefore, the reset generating circuit section 35 does not transmit the reset signal RESET to the logic circuit section 21 even if the power supply voltage is lowered when data is returned from the contactless IC card 1 to the reader/writer 2. Since the reset generating circuit section 35 does not transmit the reset signal RESET, the contactless IC card 1 can continuously return the data to the reader/writer 2.

The operation of the contactless IC card system according to the embodiment will be described hereinafter with reference to FIG. 6 which is a waveform diagram of individual signals in data communications. When data is returned from the contactless IC card 1 to the reader/writer 2, the logic circuit section 21 changes the return signal TXDATA to be transmitted to the modulator circuit 34 from the H level to the L level, as stated above. In this embodiment, during a period in which the return signal TXDATA is at the L level, the coil terminals 36 and 37 are connected to each other through the modulation factor adjusting resistor 81 shown in FIG. 3, and therefore, the voltage between the coil terminals 36 and 37 is decreased. After the voltage between the coil terminals 36 and 37 are rectified by the rectifier circuit 30, the voltage becomes a power supply voltage by the power supply voltage circuit 31, and the power supply voltage is supplied to the entire LSI 11. Therefore, during a period in which the return signal TXDATA is at the L level, if the resistance value of the modulation factor adjusting resistor 81 is large, the power supply voltage Vdd decreases from Vdd0 (Vdd0=5.0 V) to Vdd1 (Vdd1=4.5 [V]) as indicated by the straight line (1) in FIG. 6. If the resistance value of the modulation factor adjusting resistor 81 is small, the power supply voltage Vdd decreases from Vdd0 to Vdd2 (Vdd2=3.0 [V]) as indicated by the straight line (2) in FIG. 6.

The reset generating circuit section 35 includes a reset detection lower limit voltage Vreset. When the power supply voltage Vdd is lower than the reset detection lower limit

voltage Vreset, the reset signal RESET transitions to the H level. The reset generating circuit section Vreset must be lower than 4.5 [V]. In other words, when data is returned from the contactless IC card 1 to the reader/writer 2 as the contactless IC card 1 and the reader/writer 2 are spaced apart from each other, the power supply voltage Vdd is small, and if the reset detection lower limit voltage Vreset is 4.5 [V], the reset signal RESET is at the H level. At that time, the operation of the LSI 11 stops, thereby making it impossible to perform data communications between the contactless IC card 1 and the reader/writer 2. Therefore, in order to keep the state where data communications between the contactless IC card 1 and the reader/writer 2 can be performed without making the reset signal RESET at the High level even when the power supply voltage Vdd is small, the reset detection lower limit voltage Vreset included in the reset generating circuit section 35 must be decreased.

For example, suppose a case where no data at all is being exchanged between the contactless IC card 1 and the reader/writer 2, and the reset detection lower limit voltage Vreset of the reset generating circuit 35 is lowered to Vre2 (3.0 [V] or less). When the data communications between the contactless IC card 1 and the reader/writer 2 is not performed, the operation of the non-volatile memory circuit section 22 should be stopped by setting the switch signal SW to be at the H level. However, the logic circuit section 21 transmits a control signal Ctrl to the non-volatile memory circuit section 22, and therefore, the non-volatile memory circuit section 22 operates. The logic circuit section 21 typically includes only logic gates, and operates normally even if the power supply voltage Vdd drops to about 3.0 [V]. However, the non-volatile memory circuit section 22 includes not only logic gates but also memory cells, etc. Therefore, if the non-volatile memory circuit section 22 is activated with the power supply voltage Vdd having dropped to about 3.0 [V], the write time to memory cells of the non-volatile memory circuit section 22, etc., will not be as prescribed, whereby a normal operation is no longer be guaranteed. Thus, the design needs to be such that the non-volatile memory circuit

section 22 is not activated when the power supply voltage Vdd drops to about 3.0 [V].

In view of the above problems, the contactless IC card system according to the embodiment is characterized in that when the data is returned from the contactless IC card 1 to the reader/writer 2, the non-volatile memory circuit section 22 is not allowed to operate, the logic circuit section 21 buffers the data to be returned, and the return of the data is performed only by allowing the logic circuit section 21 to operate.

In this way, the function of stopping the operation of the non-volatile memory circuit section 22 and decreasing the reset detection lower limit voltage of the reset generating circuit section 35 only when the return of the data can be performed from the contactless IC card 1 and the reader/writer 2 is added into the IC card system. Therefore, communication distance between the contactless IC card and the reader/writer can be extended, thereby ensuring stable data communications.

The contactless IC card system according to the embodiment, as shown in FIG. 2, has a function of transmitting the switch signal SW from the logic circuit section 21 to the reset generating circuit section 35 in order to decrease the reset detection lower limit voltage Vreset included in the reset generating circuit section 35. Only during the period in which the switch signal SW is at the H level, the reset detection lower limit voltage of the reset generating circuit section 35 drops from Vrel (=about 4.5 [V]) to Vre2 (≤Vdd2 (=about 3.0 [V])). Thus, only when the switch signal SW is at the H level, the return of data can be performed from the contactless IC card 1 to the reader/writer 2.

The configuration of the reset generating circuit section 35 will be described hereinafter with reference to FIG. 5. Resistors 43, 44, and 45 are resistors having resistance values R1, R2, and R3, respectively, and dividing the power supply voltage to decrease the power supply voltage. The comparator 47 compares a voltage VR at the node between the resistors 44 and 45 with an output voltage Vref of a reference voltage generating circuit. A bandgap reference

voltage generating circuit is generally used as a reference voltage generating circuit 46. In the embodiment of the present invention also, a bandgap reference voltage generating circuit is used. The output voltage Vref of the bandgap reference voltage generating circuit 46 is about 1.2V. The reference voltage generating circuit can be applicable to the embodiment of the present invention no matter what value the output voltage of the reference voltage generating circuit has. The switch signal SW which indicates the period in which the data is returned from the contactless IC card 1 to the reader/writer 2 is input to a gate of a reset detection lower limit voltage Vreset setting transistor 42 through an inverter 41 as shown in FIG 5. Where the switch signal SW is at the H level, the voltage at the node between the R1 and R2 is the power supply voltage Vdd. If the reset detection lower limit voltage Vreset (=Vre1) where the switch signal SW is at the L level is 4.5 [V], the reset detection lower limit voltage Vreset (=Vre2) where the switch signal SW is at the H level is 3.0 [V], the output voltage Vref of the reference voltage generating circuit 46 is 1.2 V, and R1+R2+R3=1 [MΩ], the resistance values R1, R2 and R3 of the resistors 43, 44, and 45 can obtained by solving the set of simultaneous equations of Expressions 1 to 3 below.

$$R1+R2+R3=1000\ [k\Omega] \qquad \text{Exp. 1}$$

$$4.5/(R1+R2+R3)=1.2/R3 \qquad \text{Exp. 2}$$

(the value of the current flowing through the resistor of the reset generating circuit 35 when the switch signal SW is at the L level)

$$3.0/(R2+R3)=1.2/R3 \qquad \text{Exp. 3}$$

(the value of the current flowing through the resistor of the reset generating circuit 35 when the switch signal SW is at the H level)

Based on Expressions 1 to 3 above, the resistance values of the resistors 43, 44, and 45 are as follows: R1=333.33 [kΩ], R2=400.00 [kΩ] and R3=266.67 [kΩ].

Therefore, where the switch signal SW is at the L level, the reset detection lower limit

voltage Vreset is Vre1=4.5 [V], and the resistor of the reset generating circuit 35 is a series of resistors 43, 44, and 45. When the voltage VR at the node between the resistor 44 and the resistor 45 is lower than 1.2V (i,e., when the power supply voltage Vdd is lower than Vre1=4.5 [V]), the reset signal RESET transitions from the L level to the H level. When the switch signal SW is at the H level, the reset detection lower limit voltage Vreset is Vre2=3.0 [V], and the resistor of the reset generating circuit 35 is a series of resistors 44 and 45. When the voltage VR is lower than 1.2 V (when the power supply voltage Vdd is lower than Vre2=3.0 [V]), the reset signal RESET transitions from the L level to the H level.

On the contrary, in order to set the reset detection lower limit voltage Vreset to be Vre1=4.5 [V] or Vre2=3.0 [V], the resistance values of the resistors 43, 44, and 45 can be set to R1=333.33 [kΩ], R2=400.00 [kΩ], and R3=266.67 [kΩ], respectively, with a circuit configuration as shown in FIG. 5.

In this way, in the reset generating circuit 35 regarding the embodiment, a plurality of resistors are connected together in series, the reset detection lower limit voltage Vreset setting transistor 42 is inserted as shown in FIG. 5, and the number of resistors that decrease the power supply voltage Vdd is controlled based on the state of the switch signal SW. Therefore, the reset generating circuit section 35 of the embodiment has a function of decreasing the reset detection lower limit voltage Vreset optionally by increasing the voltage VR at the node between the resistors 44 and 45 optionally when the switch signal SW is transmitted from the logic circuit section 21. In order to change the voltage VR at the node between the resistors 44 and 45, the resistance values 43 to 45 are merely changed. Therefore, the voltage VR can easily be changed.

In the reset generating circuit section 35 of the embodiment, instead of determining the two different reset detection lower limit voltages Vre1 and Vre2 as described above, the reset signal RESET is set to be at the L level whenever the switch signal SW is transmitted. thereby

making it possible to maintain data communications between the contactless IC card 1 and the reader/writer 2 as the above described means.

Next, the change of the power supply voltage will be described when the return of data from the contactless IC card 1 to the reader/writer 2 is completed. FIG. 7 is an enlarged view showing signal waveforms observed when data is exchanged between the contactless IC card 1 and the reader/writer 2. During the period in which the return signal TXDATA is at the L level, the voltage between the coil terminals 36 and 37 is decreased by the modulator circuit 34 to Vdd2. After the return of data is completed, the return signal TXDATA is brought from the L level to the H level, and the voltage between the coil terminals 36 and 37 increases toward the Vdd0 level, and the power supply voltage Vdd increases from Vdd2 toward Vdd0 along with the voltage increase.

However, the rate at which the power supply voltage Vdd increases varies depending on capacitors parasitically included within the LSI 11 or capacitors added thereto. Specifically, when the internal capacitance of the LSI 11 is larger, the power supply voltage Vdd starts increasing slowly when the return of data from the contactless IC card 1 to the reader/writer 2 is completed, as indicated by the solid line (2) in FIG. 7. Therefore, if there is a small time difference between when the switch signal SW sent from the logic circuit section 21 to the reset generating circuit 35 transitions from the H level to the L level and when the return signal TXDATA sent from the logic circuit section 21 to the modulator circuit 34 transitions to the H level, the reset detection lower limit voltage Vreset of the reset generating circuit 35 rises to Vre1, as indicated by the dotted line (5) in FIG. 7, before the power supply voltage Vdd sufficiently returns to the voltage level Vdd0. As a result, the reset generating circuit 35 generates the reset signal RESET, whereby it is no longer possible to perform data communications between the contactless IC card 1 and the reader/writer 2.

The logic circuit section 21 according to the embodiment of the present invention

delays the fall of the switch signal SW, as indicated by the dotted line (3) in FIG. 7. However, if the fall of the switch signal SW is delayed excessively, the operation of the non-volatile memory circuit section 22 starts while the LSI 11 performs the internal operation. Thus, the logic circuit section 21 can delay the fall of the switch signal SW by a period longer than the period in which the return signal TXDATA is at the L level with respect to the rise of the return signal TXDATA sent to the modulator circuit 34 as shown in FIG. 7. To be exact, the modulation frequency is 848 kHz in the international standard "ISO/IEC 14443 Type B" for contactless IC cards, and therefore the fall of the switch signal SW can be delayed by a period greater than or equal to 1.18 [μs/2], i.e., 590 [ns].

The logic circuit section 21 according to the embodiment is configured so as to stops transmitting the switch signal SW with timings as described above by using the clock signal CLK transmitted from the clock generating circuit 32.

Further, other than the reset detection lower limit voltage Vreset, a reset detection upper limit voltage V'reset can be provided as a reset detection voltage in the contactless IC card system of the embodiment. This will be described with reference to FIG. 8 which is a waveform diagram of showing the relationship among the reset detection lower limit voltage Vreset, the reset detection upper limit voltage V'reset, and the power supply voltage Vdd.

When data is returned from the contactless IC card 1 to the reader/writer 2 (during the period in which the return signal TXDATA transmitted from the logic circuit section 21 to the modulator circuit 34 is at the L level), if the resistance value of the modulation factor adjusting resistor 81 is low, the power supply voltage Vdd decreases from Vdd0 to Vdd2. As is synchronized with the decrease of the power supply voltage Vdd, the reset detection upper limit voltage V'reset having voltages Vre3 and Vre4 which are higher than the power supply voltages Vdd0 and Vdd2 is determined. When the power supply voltage Vdd is larger than the determined reset detection upper limit voltage V'reset, the reset signal RESET transitions the L

level to the H level, thereby imparting the reset generating circuit section 35 a function of stopping the data communications between the contactless IC card 1 and the reader/writer 2. Specifically, a circuit for adding one inverter to the output section of a circuit having a configuration similar to the reset generating circuit 35 of FIG. 5 is parallely-connected to the original reset generating circuit section 35. In this way, as well as a series of resistors in the new reset generating circuit section of FIG. 5, the number of resistors for decreasing the power supply voltage Vdd is changed, whereby the two reset detection upper limit voltages Vre3 and Vre4.

The contactless IC card 1 with this function has an effect of improving safety as described below. For example, if a third person attempts, with malicious intent, to externally power the LSI 11 of this variation to read out, or overwrite, signals inside the LSI 11 and data stored in the non-volatile memory circuit section 22, the third person needs to externally supply a voltage that can be used in place of the power supply voltage Vdd. The reset generating circuit section 35 of the embodiment has the reset detection lower limit voltage Vreset and the reset detection upper limit voltage V'reset. Therefore, a power supply voltage in place of the power supply voltage Vdd needs to be always higher than the reset detection lower limit voltage Vreset and lower than the reset detection upper limit voltage V'reset so that the reset signal RESET will not be generated. It is very difficult to have such an external power supply voltage always adjusted so that the reset signal RESET will not be generated. Thus, with the contactless IC card system of the embodiment, it is easy to sufficiently improve the security of the LSI 11 without complicating the circuit configuration of the reset generating circuit 35.

In this way, the semiconductor integrated circuit of the present invention having the function of decreasing the detection voltage level of the reset generating circuit section during modulation is useful as a semiconductor integrates circuit for contactless IC cards which is given the electric power from the reader/writer 2, and which generates the power supply voltage Vdd

therein.

While a voltage doubler rectifier is used as the rectifier circuit 30 in the above embodiment, the present invention may use a rectifier circuit that rectifies radio waves by means of a full-wave rectifier circuit or a half-wave rectifier circuit. The voltage doubler rectifier has a feature of having a voltage value, obtained after rectification, larger than values of other rectifier circuits. While a circuit that modulates the voltage between the coil terminals 37 and 37 is used as the modulator circuit 34 of the above embodiment, a modulator circuit that modulates the power supply voltage Vdd can also be used.

[Industrial Applicability]

The semiconductor integrated circuit of the present invention has a function of decreasing detection voltage of the reset generating circuit when data is returned from the contactless IC card to the reader/writer, and is useful as a semiconductor integrated circuit for contactless IC cards which is given the electric power from the reader/writer 2, and generates the power supply voltage Vdd therein. Thus, the present invention is useful as a contactless type information medium which includes the semiconductor integrated circuit therein, and the like.

[Brief Description of Drawings]

[FIG. 1] FIG. 1 is a schematic diagram of a contactless IC card system.

[FIG. 2] FIG. 2 is a diagram showing a block configuration example of a LSI 11.

[FIG. 3] FIG. 3 is a diagram showing a configuration diagram of a modulator circuit 34 and a rectifier circuit 30 of a contactless IC card 1.

[FIG. 4] FIG. 4 is a correlation diagram between the magnetic field intensity and the modulation factor.

[FIG. 5] FIG. 5 is a diagram showing a configuration example of a reset generating circuit 35.

[FIG. 6] FIG. 6 is a waveform diagram (1) of individual signals.

[FIG. 7] FIG. 7 is a waveform diagram (2) of individual signals (enlarged view).

[FIG. 8] FIG. 8 is a waveform diagram (3) of individual signals.

[Description of the Reference Numerals]

1	Contactless IC card (data carrier)
2	Reader/writer
3	Host device
4	Antenna coil
5	Electromagnetic wave
11	LSI
12	Antenna coil
13	Tuning capacitor
20	Analog circuit section
21	Logic circuit section
22	Non-volatile memory circuit section
30	Rectifier circuit
31	Power supply circuit
32	Clock generating circuit
33	Demodulator circuit
34	Modulator circuit
35	Reset generating circuit
36	Coil terminal
37	Coil terminal
41	Inverter
42	Reset detection lower limit voltage Vreset setting transistor
43	Reset detection lower limit voltage adjusting resistor
44	Reset detection lower limit voltage adjusting resistor

45	Reset detection lower limit voltage adjusting resistor
46	Reference voltage generating circuit
47	Comparator
81	Modulation factor adjusting resistor
82	Modulation transistor
83	Diode
84	Diode

[Name of the Document] Abstract

[Abstract]

[Problems] The present invention has an object to provide a semiconductor integrated circuit that ensures the miniaturization of the size of a contactless IC card (contactless type information medium) having a simple configuration and the circuit therein, and that achieves rapid and stable communications.

[Solution] The semiconductor integrated circuit of the present invention and the contactless type information medium including the semiconductor integrated circuit therein does not generate a reset signal to a logic circuit section 21 from a reset generating circuit section 35 due to the decrease of the power supply voltage by an operation of a load modulation type modulator circuit when data is transmitted from the contactless IC card to a data carrier. Therefore, it is possible to extend the reading range between the contactless IC card and the reader/writer, thus ensuring a stable operation of the entire semiconductor integrated circuit without having big circuits. Thus, the semiconductor integrated circuit of the present invention makes it possible to devise contactless IC cards of the proximity type (reading range: 0 to 10 cm) expected to be widespread in the near future.

[Selected Figure] Figure 2

【書類名】図面 [Name of the Document] Drawings

【図1】 [Figure 1]

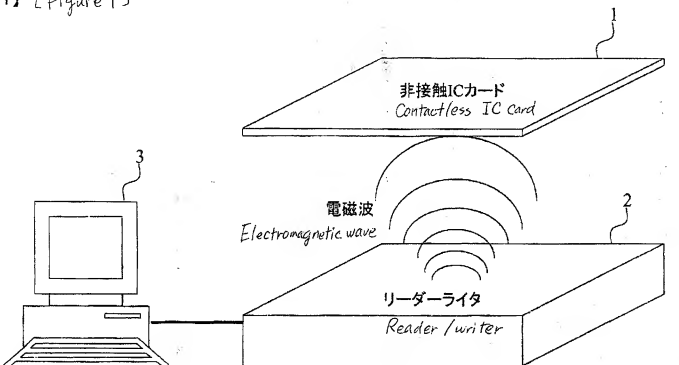

図1 非接触型ICカードシステムの概要図

Figure 1 Schematic diagram of contactless IC card system

【図2】[Figure 2]

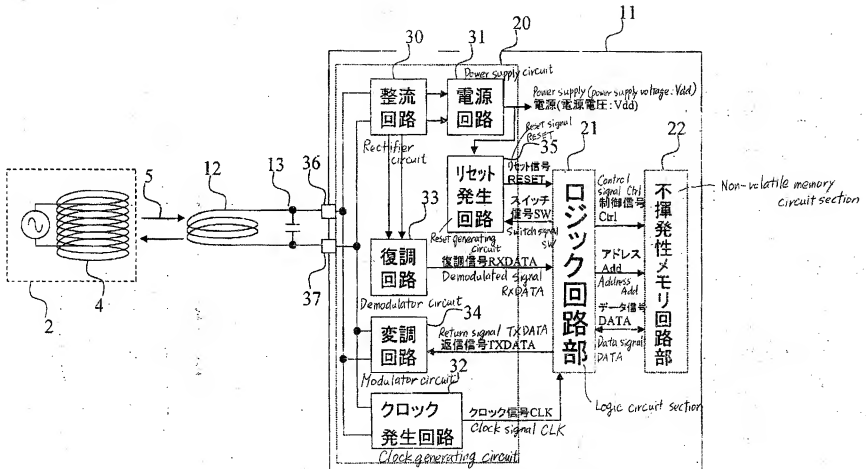

図2 LSI 11のブロック構成図

Figure 2 Block configuration diagram of LSI 11

【図3】[Figure 3]

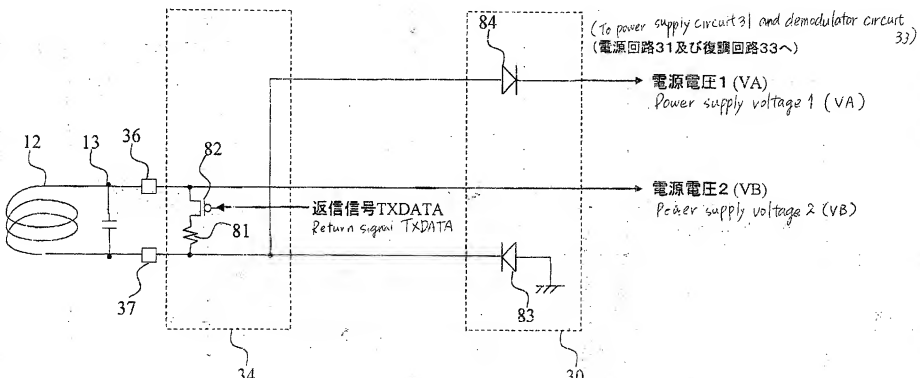

図3 非接触ICカード1の変調回路34と整流回路30の構成図

Figure 3 Configuration diagram of modulator circuit 34 and rectifier circuit 30 of contactless IC card 1

【図4】[Figure 4]

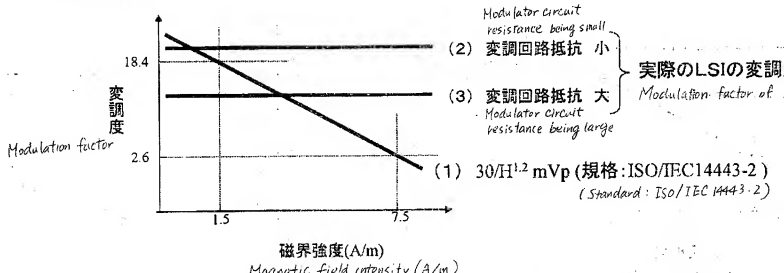

図4 磁界強度と変調度との相関図

Figure 4 Correlation diagram of magnetic field intensity and modulation factor

【図5】[Figure 5]

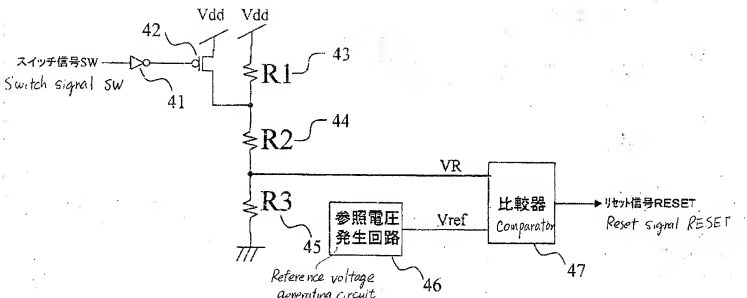

図5 リセット発生回路35の構成例

Figure 5 Configuration example of reset generating circuit 35

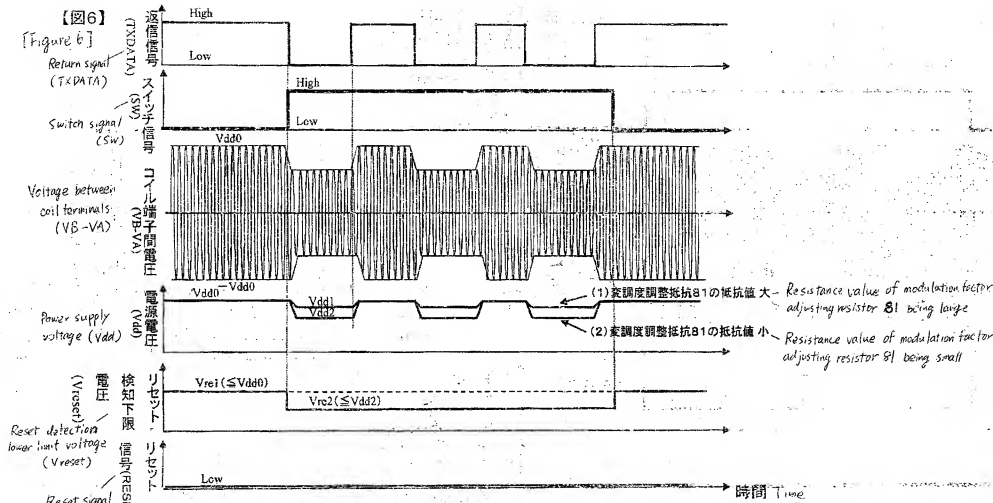

図6 各信号波形図1

Figure 6 Waveform diagram 1 of individual signals

【図7】[Figure 7]

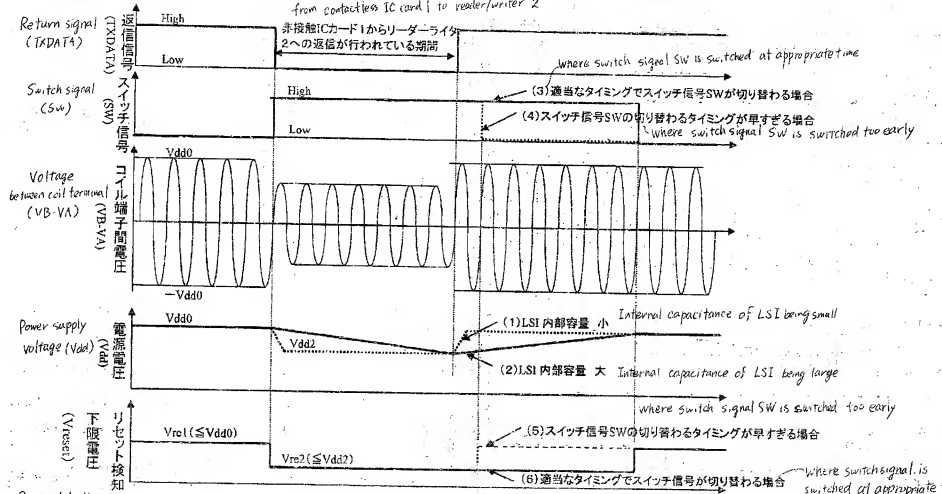

図7 各信号波形図2(拡大図)

Figure 7 Waveform diagram 2 of individual signals (enlarged view)

【図8】[Figure 8]

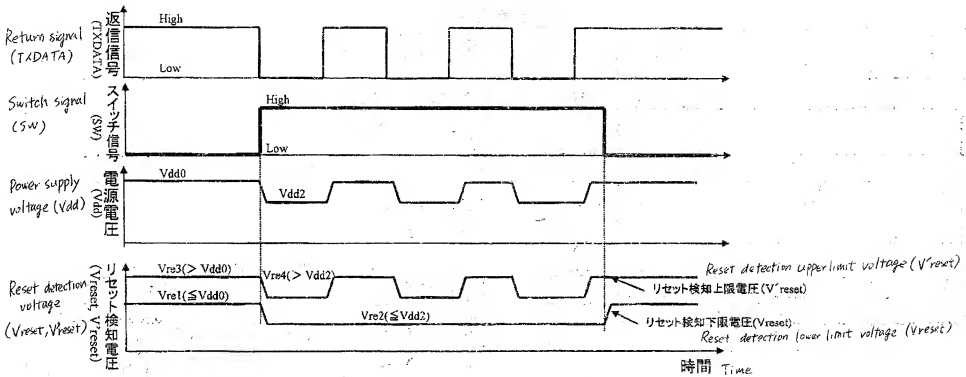

図8 各信号波形図3

Figure 8 Waveform diagram 3 of individual signals